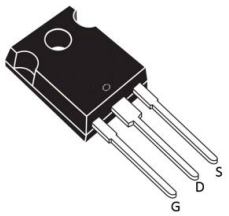
Silicon N-Channel Power MOSFET

General Description :

The HMP400N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is TO-247, which accords with the RoHS standard.

V_{DSS}	40	V
I_D	400	A
P_D	500	W
$R_{DS(ON)type}$	1.4	mΩ

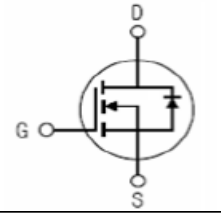
TO-247



Features :

- $R_{DS(ON)}$ <1.65mΩ @ V_{GS}=10V (Typ1.4mΩ)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Inner Equivalent Principium Chart



Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Absolute (Tc= 25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	40	V
I_D	Continuous Drain Current	400	A
I_{DM}	Pulsed Drain Current	1250	A
V_{GS}	Gate-to-Source Voltage	±20	V
P_D	Power Dissipation	500	W
E_{AS}	Single pulse avalanche energy	2000	mJ
T_J , T_{stg}	Operating Junction and Storage Temperature Range	175 , −55 to 175	℃

Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=32V, V_{GS}= 0V,T_a=25℃	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+20V	--	--	0.1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-20V	--	--	-0.1	μA

ON Characteristics[a3]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=80A	--	1.4	1.65	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	--	4.0	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V,V_{DS}=25V f=1.0MHz	--	10.8	--	nF
C_{oss}	Output Capacitance		--	1.6	--	
C_{rss}	Reverse Transfer Capacitance		--	0.88	--	

Resistive Switching Characteristics[a4]						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=26V,I_D=200A V_{GS}=10V,R_G=2.1Ω,R_L=0.5Ω	--	30	--	ns
t_r	Rise Time		--	30	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	155	--	
t_f	Fall Time		--	43	--	
Q_g	Total Gate Charge	V_{DD}=20V, I_D=200A V_{GS}=10V	--	158	--	nC
Q_{gs}	Gate to Source Charge		--	38	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	42	--	

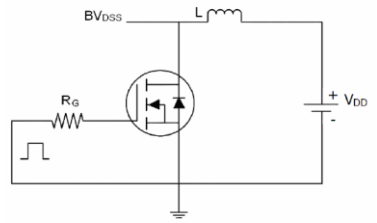
Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current [a2](Body Diode)		--	--	400	A
V_{SD}	Diode Forward Voltage[a3]	I_S=200A,V_{GS}=0V	--	--	1.2	V
t_{rr}	Reverse Recovery Time	I_S=200A,T_j=25℃	--	85	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/μs V_{GS}=0V	--	70	--	nC

Symbol	Parameter	Typ.	Units
$R_{\theta JC}$	Junction-to-Case[a2]	0.32	℃/W

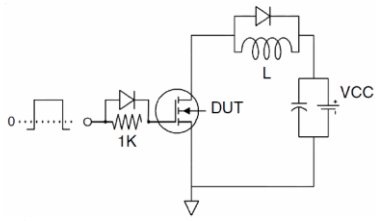
[a1] : Repetitive Rating: Pulse width limited by maximum junction temperature.
[a2] : Surface Mounted on FR4 Board, t≤10sec.
[a3] : Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%.
[a4] : Guaranteed by design, not subject to production

Test circurt

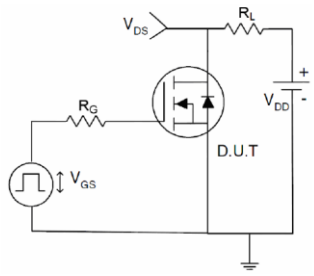
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Characteristics Curve :

Fig. 1. Output Characteristics @ T_J = 25ºC

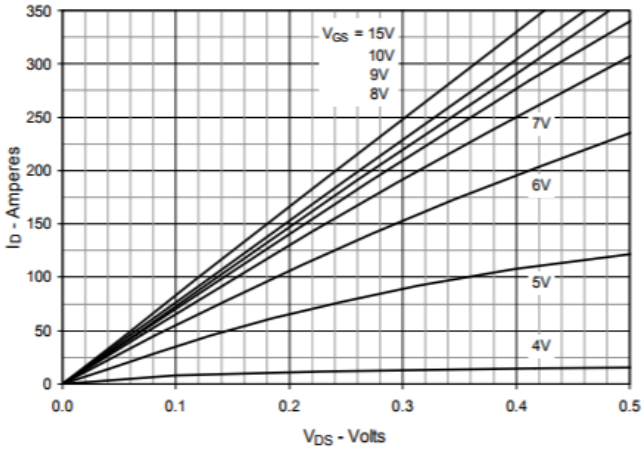


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

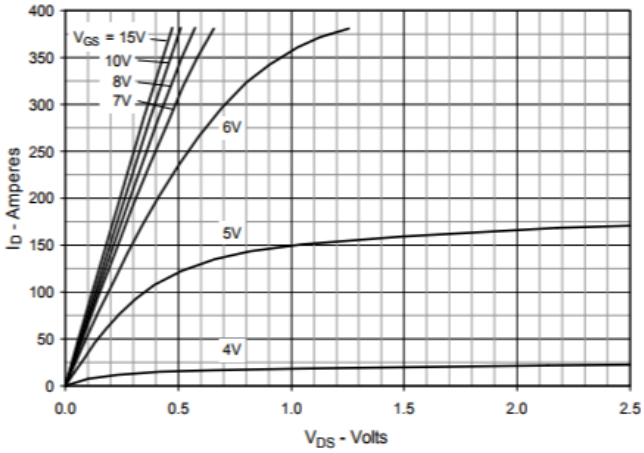


Fig. 3. Output Characteristics @ T_J = 150ºC

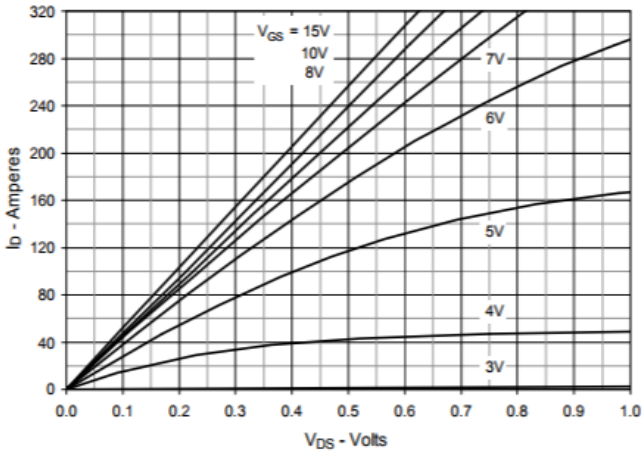


Fig. 4. $R_{DS(on)}$ Normalized vs. Junction Temperature

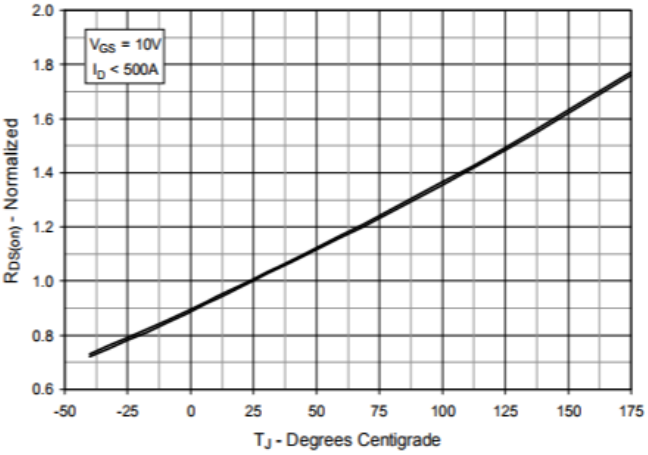


Fig. 5. $R_{DS(on)}$ Normalized vs. Drain Current

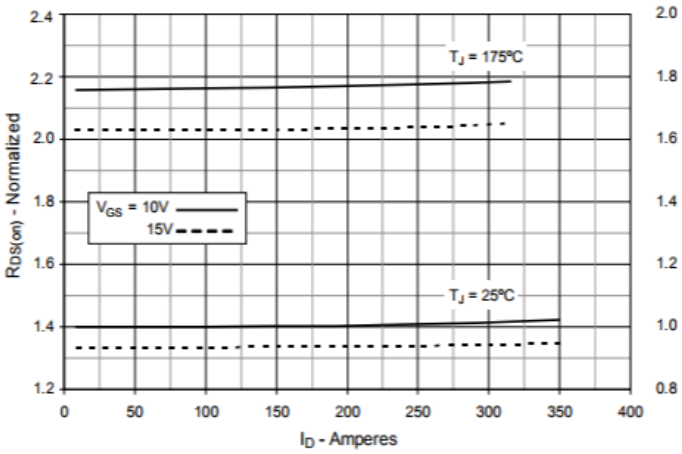


Fig. 6. Drain Current vs. Case Temperature

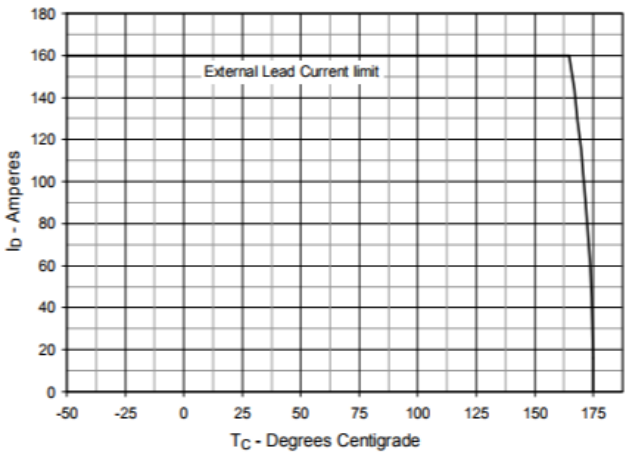


Fig. 7. Input Admittance

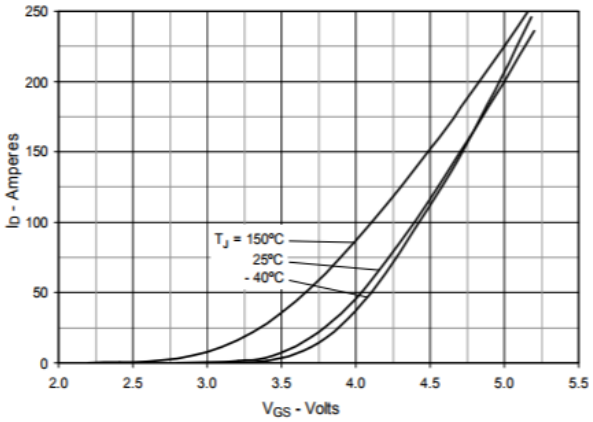


Fig. 8. Transconductance

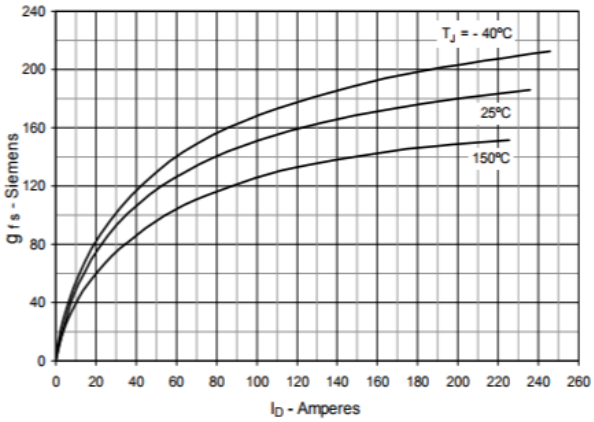


Fig. 9. Forward Voltage Drop of Intrinsic Diode

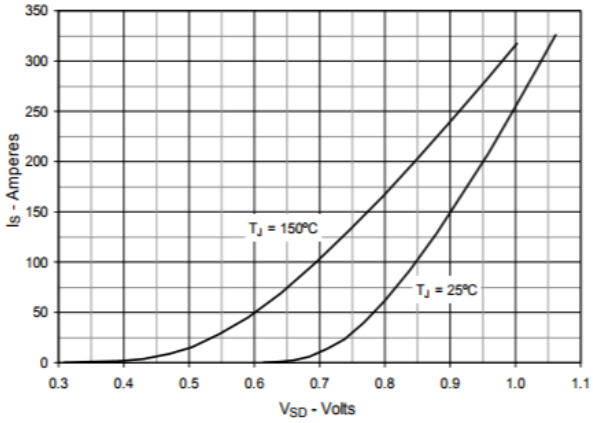


Fig. 10. Gate Charge

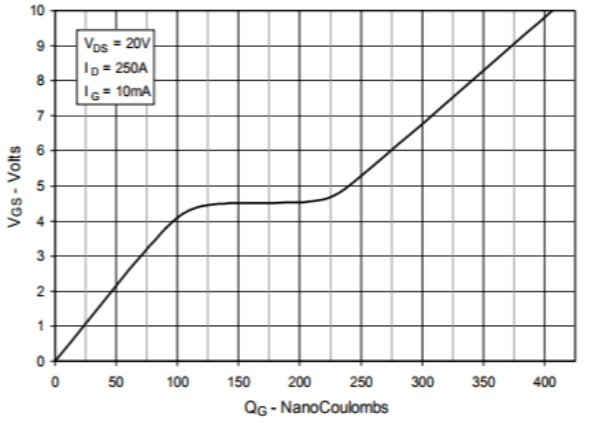


Fig. 11. Capacitance

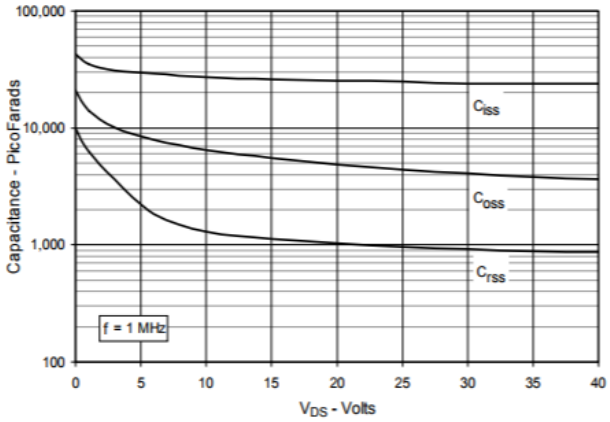


Fig. 12. Forward-Bias Safe Operating Area

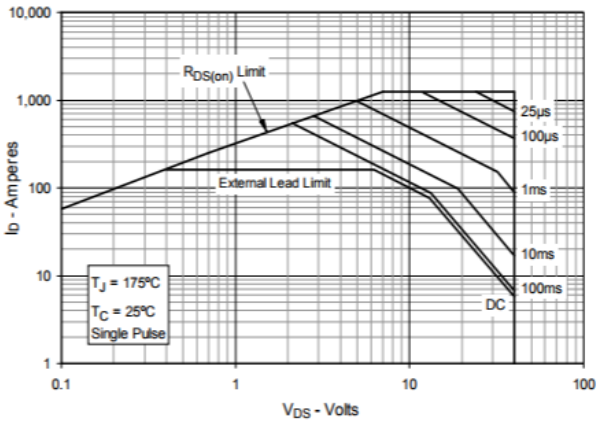


Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature

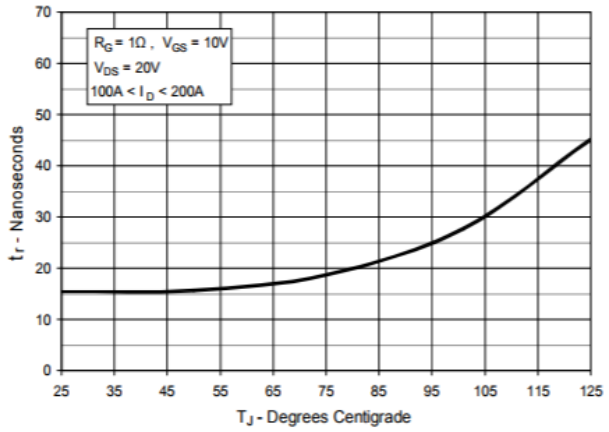


Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current

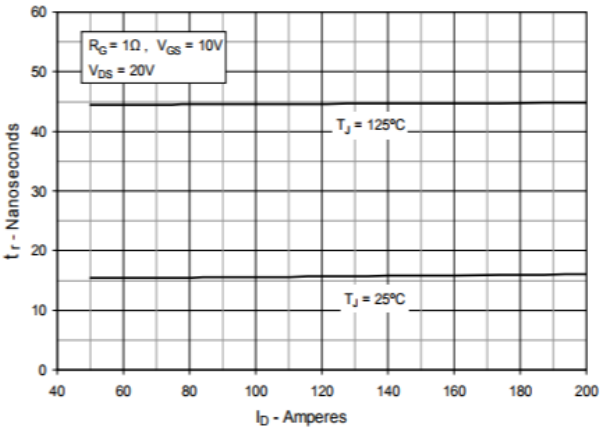


Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance

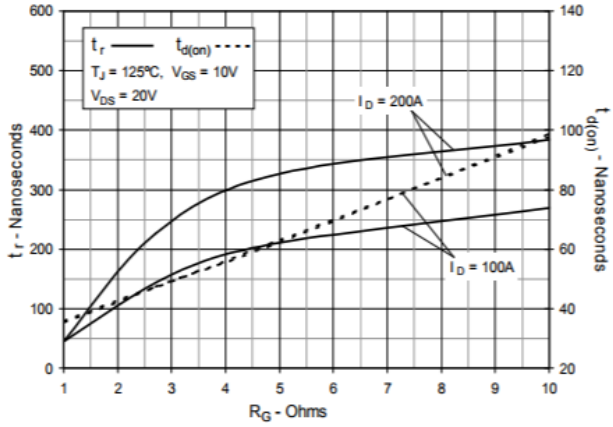


Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature

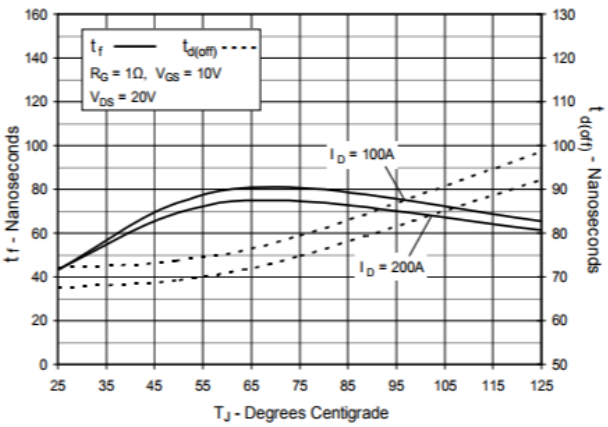


Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current

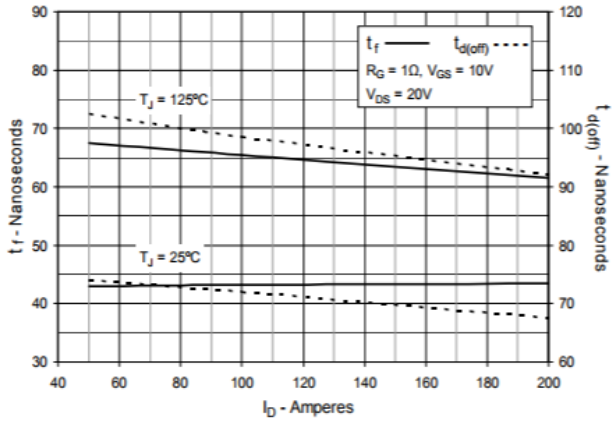


Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance

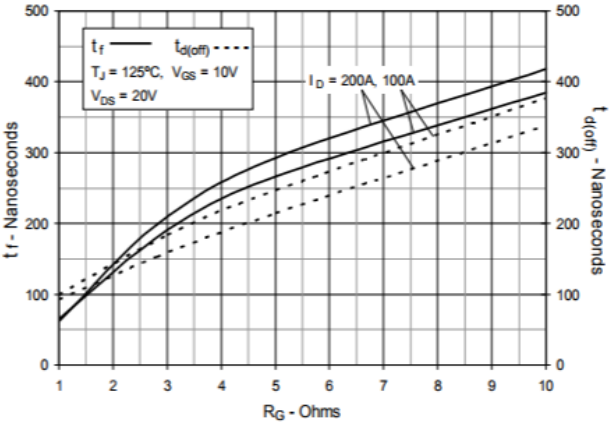


Fig. 19. Maximum Transient Thermal Impedance