General Description :

HMM44N100, the silicon N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is Sot-227B, which accords with the RoHS standard.

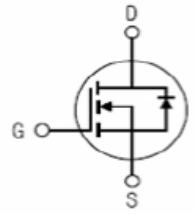
$V_{DSS}(T_C=150℃)$	1000	V
I_D	44	A
$P_D(T_C=25℃)$	960	W
$R_{DS(ON)MAX}$	220	mΩ

SOT-227B

Features :

- Fast Switching
- ESD Improved Capability
- 100% Single Pulse avalanche energy Test

Inner Equivalent Principium Chart



Applications:

- Power switch circuit of POWER

Absolute (Tc=25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	1000	V
I_D	Continuous Drain Current	44	A
	Continuous Drain Current T_C=100 °C	31	A
I_{DM}[a1]	Pulsed Drain Current(pulse width limited by T_{JM})	176	A
V_{GS}	Gate-to-Source Voltage	±40	V
E_{AS}	Single Pulse Avalanche Energy	4500	mJ
E_{Ar}[a1]	Avalanche Energy ,Repetitive	60	mJ
I_{AR} [a1]	Avalanche Current	38	A
dv/dt[a2]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	960	W
	Derating Factor above 25°C	7.68	W/℃
T_J , T_{stg}	Operating Junction and Storage Temperature Range	150 , −55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

Caution Stresses greater than those in the "Absolute Maximum Ratings" may cause permanent damage to the device

Thermal Characteristics

Symbol	Parameter	Rating	Units
R_{thJC}	Thermal Resistance, Junction-to-Case	0.13	℃/ W
R_{thcs}	Thermal Resistance, Case to heatsink	0.05	℃/ W

Electrical Characteristics (Tc= 25℃ unless otherwise specified) :

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	1000	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=1000V, V_{GS}=0V,T_a=25℃	--	--	1.0	μA
		V_{DS}=800V, V_{GS}=0V,T_a=125℃	--	--	100	
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=-30V	--	--	-100	nA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=22A	--	150	220	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	2.0	--	4.0	V
g_{fs}	Forward Trans conductance	V_{DS}=15V,I_D=22A	--	50	--	S
Pulse width<380μs; duty cycle<2%.						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS}=0V V_{DS}=25V f=1.0MHz	--	14	--	nF
C_{oss}	Output Capacitance		--	1150	--	pF
C_{rss}	Reverse Transfer Capacitance		--	120	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D=22A,V_{DD}=500V V_{GS}=10V,R_g=25Ω	--	66	--	ns
t_r	Rise Time		--	60	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	120	--	
t_f	Fall Time		--	70	--	
Q_g	Total Gate Charge	I_D=22A,V_{DD}=500V V_{GS}=10V	--	450	--	nC
Q_{gs}	Gate to Source Charge		--	80	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	140	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_{SD}	Continuous Source Current (Body Diode)		--	--	44	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	176	A
V_{SD}	Diode Forward Voltage	I_S=44A,V_{GS}=0V	--	--	1.5	V
t_{rr}	Reverse Recovery Time	I_S=44A,T_j=25℃	--	560	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt=100A/μs, V_{GS}=0V	--	5.8	--	uC

a1 : Repetitive rating; pulse width limited by maximum junction temperature

a2 : I_{SD}=44A,di/dt≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve :

Fig. 1. Output Characteristics @ T_J = 25ºC

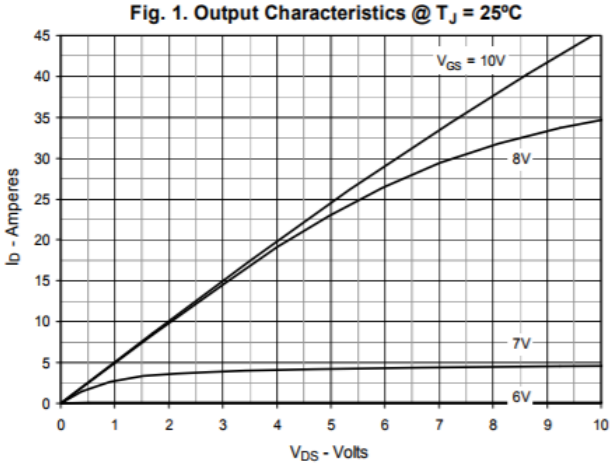


Fig. 2. Extended Output Characteristics @ T_J = 25ºC

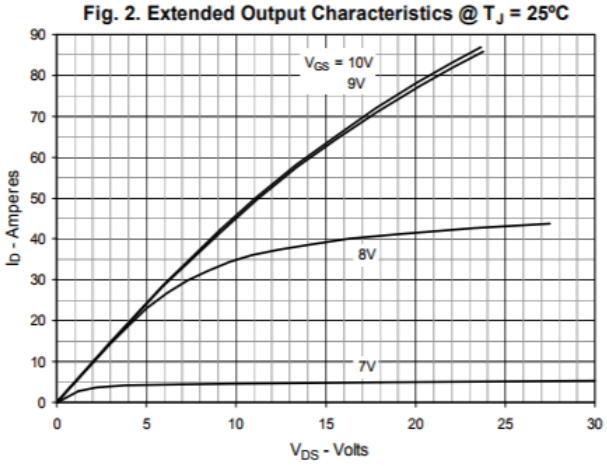


Fig. 3. Output Characteristics @ T_J = 125ºC

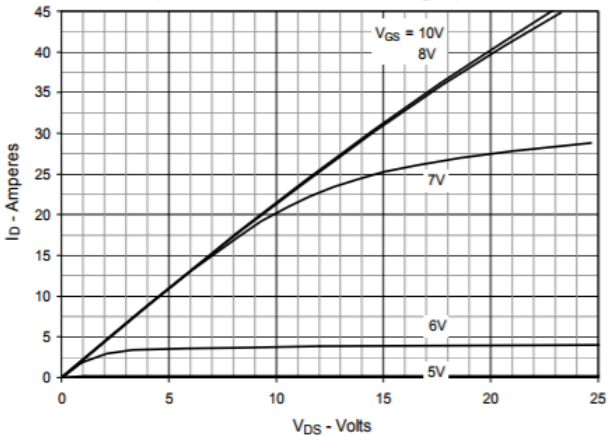


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Junction Temperature

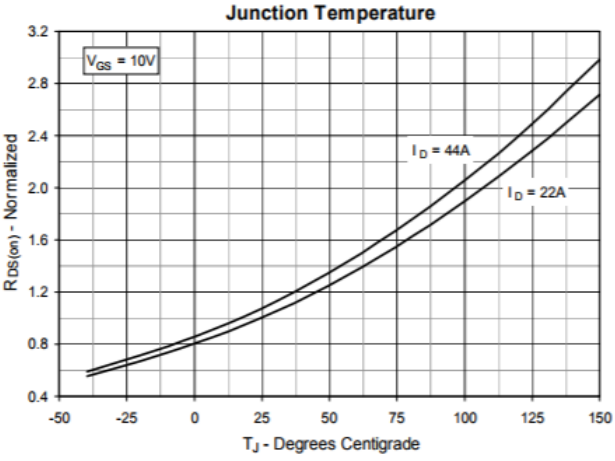


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 22A Value vs. Drain Current

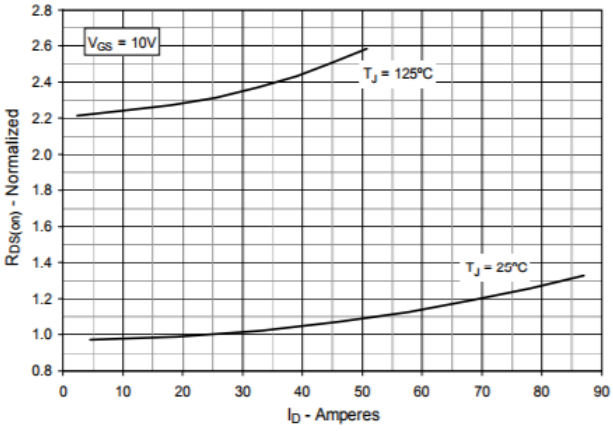


Fig. 6. Maximum Drain Current vs. Case Temperature

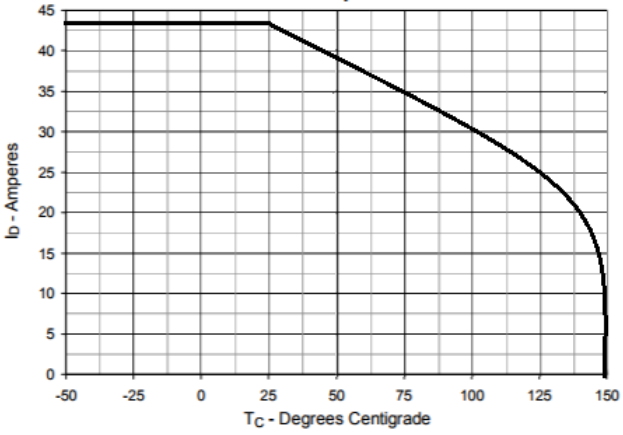


Fig. 7. Input Admittance

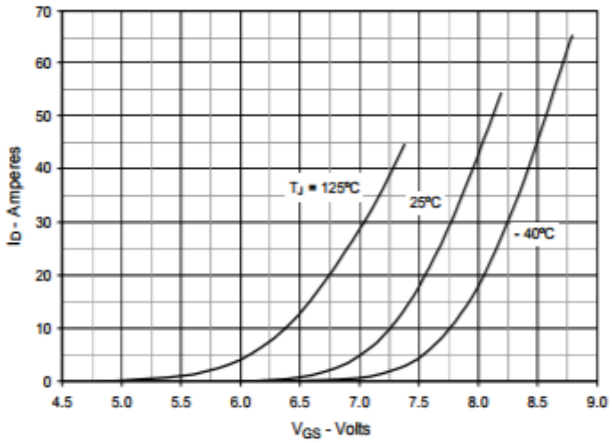


Fig. 8. Transconductance

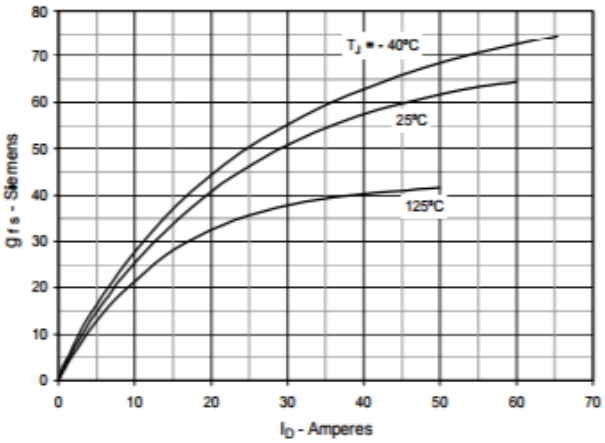


Fig. 9. Forward Voltage Drop of Intrinsic Diode

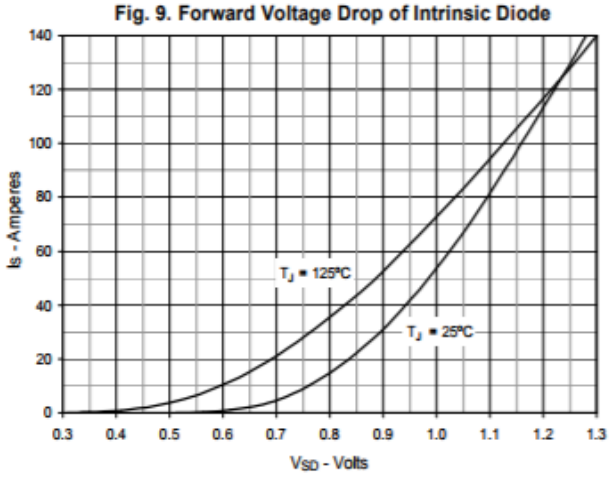


Fig. 10. Gate Charge

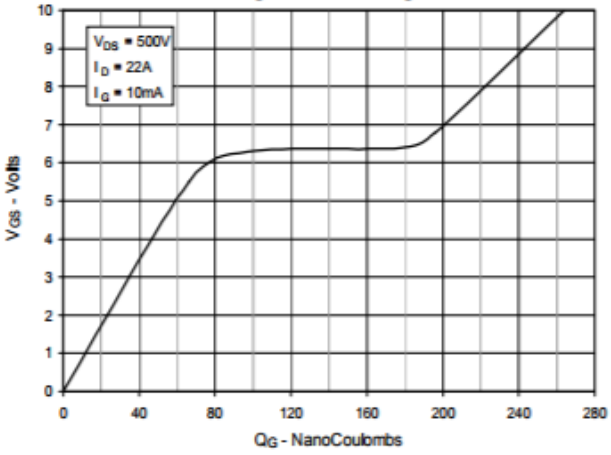


Fig. 11. Capacitance

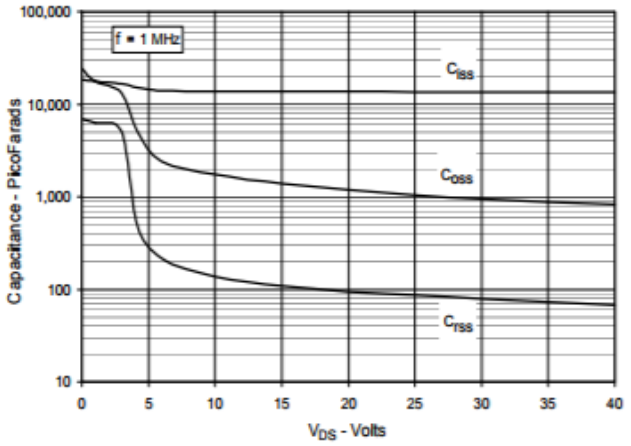


Fig. 12. Forward-Bias Safe Operating Area

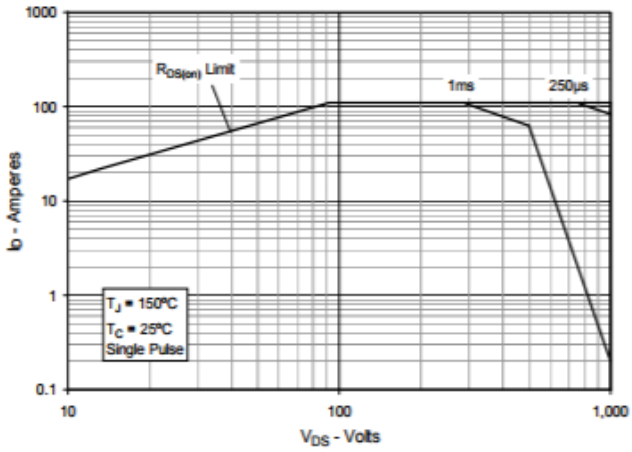


Fig. 13. Maximum Transient Thermal Impedance